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Second Generation Current Conveyor Based Floating Fractional Order Memristance Simulator and a New Dynamical System

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***Abstract*:** *In recent years, due to its non-volatile memory, non-locality, and weak singularity features, fractional calculations have begun to take place frequently in artificial neural network implementations and learning algorithms. Therefore, there is a need for circuit element implementations providing fractional function behaviors for the physical realization of these neural networks. In this study, a previously defined integer order memristor element equation is changed and a fractional order memristor is given in a similar structure. By using the obtained mathematical equation, frequency-dependent pinched hysteresis loops are obtained. A memristance simulator circuit that provides the proposed mathematical relationship is proposed. Spice simulations of the circuit are run and it is seen that they are in good agreement with the theory. Also, the non-volatility feature has been demonstrated with Spice simulations. The proposed circuit can be realized by using the integrated circuit elements available on the market. With a small connection change, the proposed structure can be used to produce both positive and negative memristance values.*

***Keywords*:** *Memristor, Memristance Simulator, Fractional Order, Circuit Implementation, ANN Realization, ANN Hardware.*

1. Introduction

Memristor is a two-terminal passive circuit element, which provides a non-linear relationship between charge and flux [1]. HP's announcement that the memristor element was physically accomplished [2] has led researchers to focus on work on the potential uses of the memristor. As a result of the researchers' study, new studies have emerged in application areas such as Analog circuit designs [3], chaotic circuits [4], sensors [5], memory devices [6] and synapse realization [7-8]. Memristor emulator circuits mostly used in artificial neural network realization because of highly similar characteristic behaviour of biologic synapses [9].

New research has shown that fractional order calculus is an effective and very useful tool, such as integer order calculus, for the design of efficient learning

algorithms [10, 11]. As an example from the studies in the literature, the fractional calculus-based Hopfield Neural Networks was proposed in 2009 by B o r o o m a n d and M e n h a j [12]. In this study, instead of the current of the capacitor element in the dynamic neuron of the Hopfield model, a current proportional to the fractional order derivative of the element voltage is explained. A new fractional adaptive learning approach, called the fractional steepest descent, was proposed in 2015 by P u et al. [13]. In this study, the learning conditions, stability, and convergence of the new approach are examined in detail. In 2017 in the study of W a n g et al. [14], the fractional gradient descent method was proposed for the backpropagation training of neural networks. In particular, the Caputo derivative is used to evaluate the fractional order gradient of the error, which is defined as the traditional quadratic energy function. The monotonicity and convergence of the approach have been studied in detail. In order to examine the performance of the proposed method, two simulations have been implemented for four different datasets. Recently, as the areas where Fractional order methods are used have started to expand, Fractional order methods have been frequently found in application areas such as signal processing [15] and image processing [16]. The fact that the fractional order capacitor element, called fractal, is used in many applications in the literature, is considered to be an indication that fractional memcapacitor will be an element used in many application areas in the future. There are various mutator circuits used in the literature to convert the fractional order memristor element into fractional order memcapacitor or meminductor [17-18].

According to studies in the literature, fractional order memristor is not only used in learning algorithms, but is also widely used in the creation of Fractional Order Neural Networks (FONN). The most common use of fractional order elements in FONN applications is the replacement of capacities in the integer order neural network circuit with fractional order capacitors [19]. In the study conducted by A r e n a, F o r t u n a , and P o r t o [20], a new network structure has been created by replacing the cells in the first layer in the Cellular Neural Network structure with fractional order cells and this network structure was used as a chaos generator. Inclusion of fractional cells in the network with appropriate joining parameters allows chaos to start in a simple two-cell system. The studies on FONNs are focused on their dynamic analysis and synchronization [21]. Another research topic in the literature is the extraction of mathematical proof of limit cycle, chaotic phenomenon formation, and investigation of complex dynamics [22-23]. In addition to these studies, many FONN structures using fractional order memristor element have been proposed [21-24]. This is because FONNs give much more effective results than integer order models in applications such as parameter estimates. The reason for this is that these structures are characterized by infinite memory.

In this study, a detailed analysis of a simulator circuit designed to implement a previously proposed fractional order memristance equation is given [25]. Thanks to the low cost fractional order memristance simulator circuit created, it will be possible to realize theoretical learning methods, neural network structures, and signal processing algorithms physically.

2. Integer order memristance simulator

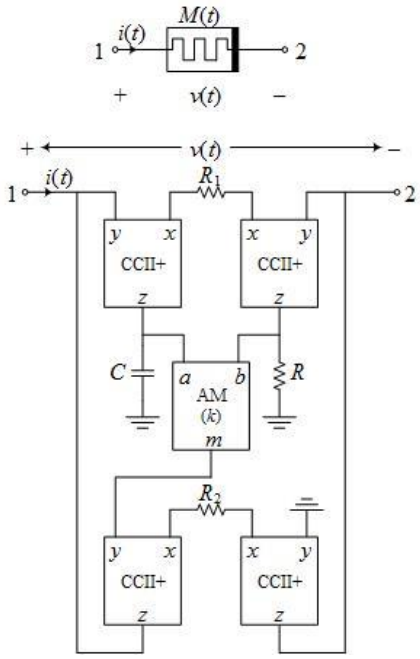


Fig. 1. Integer order memristance simulator circuit

In this study, a previously defined integer order memristance simulator circuit is taken as starting point [26]. The block-diagram of the reference circuit generated by using Current Conveyors II-generation positive type (CCII+) and Analog Multiplier (AM) is given in Fig. 1. The defining equations of CCII+ are $i_x(t) = 0$, $i_z(t) = i_y(t)$ and $v_x(t) = v_y(t)$. The defining equation of AM is $v_m(t) = kv_x(t)v_y(t)$, where k is a coefficient in V^{-1} unit. When this circuit is analysed by using the defining equations of CCII+ and AM, the memristance function is obtained in the equation

$$M(t) = \frac{v(t)}{i(t)} = \pm \frac{R_1^2 R_2 C}{k\varphi(t) R}, \tag{1}$$

where $\varphi(t)$ is the flux on the memristor element.

The characteristic fingerprint of a memristor element is defined as follows:

1. When driven by a bipolar periodic signal, the voltage-current plane must exhibit a pinched hysteresis loop;

2. From a certain critical frequency, as the frequency of the applied signal increases, the hysteresis lobe decreases, and

3. When the frequency goes to infinity, the resulting hysteresis loop should turn into a single-valued function [27].

If the values in Table 1 are selected as the element values used in the circuit, when the sinusoidal signals at 500 Hz, 1 kHz and 5 kHz frequencies and 1 V amplitude are applied to this simulator circuit, the characteristic hysteresis curves as in Fig. 2 are obtained. It is seen that these curves provide all three characteristic fingerprints of the memristor element.

Table 1. Circuit parameters used in Fig.2 integer order memristance simulator circuit

Element	R_1	R_2	R	C	k
Value	47 kΩ	10 kΩ	194 kΩ	100 nF	0.1 V^{-1}

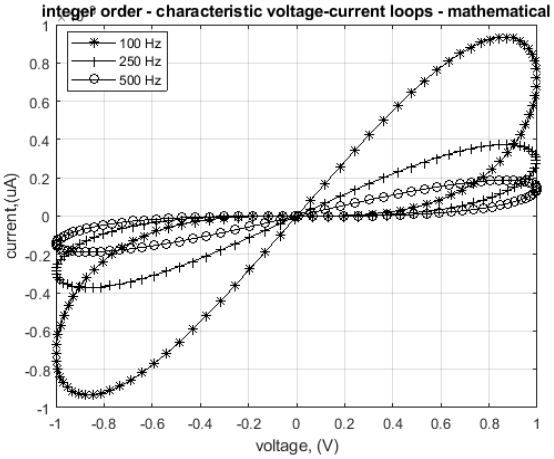


Fig. 2. Characteristic *v-i* hysteresis loops of integer order memristance simulator circuit

The aim of the study is to design a memristance value in fractional order, maintaining the basic form of this integer order simulator circuit.

3. Fractional order memristance equation

The flux $\varphi(t)$ is the first order time integral of the element voltage $v(t)$. The Laplace transform of this integral operator is

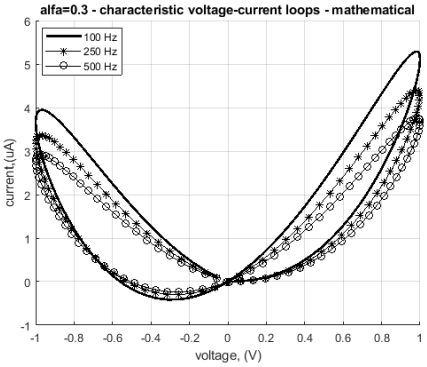
$$\Phi(s) = \frac{V(s)}{s}. \tag{2}$$

If it is desired to obtain a fractional order derivative, as seen in the next equation, α power of the denominator of the relation (2) is used:

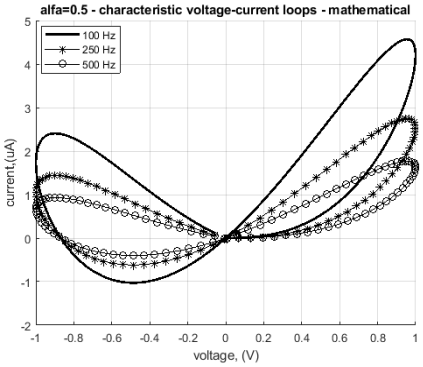
$$\Phi_f(s) = \frac{V(s)}{s^{\alpha}}, \tag{3}$$

where, α is the fractional order.

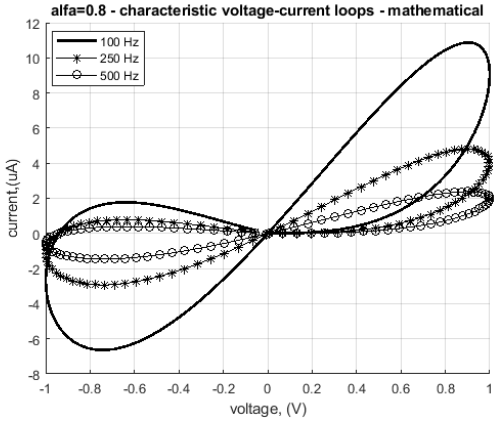
Considering the first order memristance equation in (1), it is seen that the memristance is inversely proportional to the first order flux $\varphi(t)$. All parameters except flux are constant coefficients, therefore (1) can be considered as $M(t)=K/\varphi(t)$. Since it is desired to obtain a fractional order memristance equation in the same form, the aim in this study is to obtain a memristance equation as $M_f(t)=K/\varphi_f(t)$ that is inversely proportional to fractional order flux and to realize this magnitude. The mathematically obtained pinched hysteresis loops are given in Fig. 3, with the input frequencies 100 Hz, 250 Hz and 500 Hz, for changing values of α. As seen in Fig 3, the mathematically obtained hysteresis loops using this relationship provide the fingerprints of the memristor element.



(a) α=0.3, K=38,000



(b) α=0.5, K=11,000



(c) α=0.8, K=1100

Fig. 3. Mathematically obtained characteristic pinched *v-i* hysteresis loops of fractional order memristor for changing α values

4. Fractional Order Memristance Simulator Circuit

In the circuit in Fig 1, a capacitor element is used to produce the first order flux. In order to obtain the fractional order flux with the same structure, it is necessary to add a Fractional Order Integrator (FOI) to the circuit. For Laplace transform of the FOI, first order approximation can be used:

(4a) $$\frac{1}{s^{\alpha}} \approx \frac{Bs+1}{B+s},$$

(4b) $$B = \frac{1-\alpha}{1+\alpha}, \text{ when } 0<\alpha<1.$$

A FOI circuit realizes the first order approximation given in Fig. 4 [28]. Here, μ is amplitude scaling coefficient.

AD844 integrated circuit can be used as CCII+ by leaving the w terminal open circuit. In this way, 2 types of active elements are used in the proposed circuit; AD844

CFOA integrated circuit and AD633 analog multiplier element. Thus the proposed fractional order memristance simulator circuit is obtained as in Fig 5.

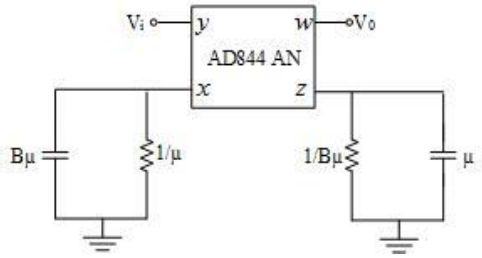
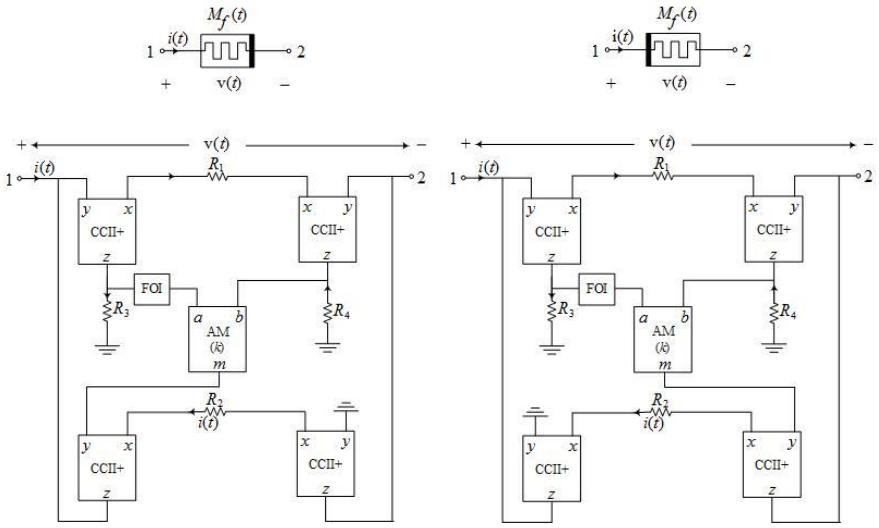


Fig. 4. FOI circuit



(a) Positive type (b) Negative type

Fig. 5. Proposed fractional order memristance simulator circuit

With a small connection change, the direction of the current flowing through the element in the circuit is changed, and the memristance value produced by the proposed circuit can be positive or negative. The value of the memristor element which is the fourth basic circuit element defined by Chua, will always be positive, but negative memristance can also be used for some applications, similar to negative resistance. The memristance equation for positive and negative memristance simulator circuits in Fig. 5 is

(5) $$M_f(t) = \pm \frac{R_1^2 R_2}{k\varphi(t) R_3 R_4}.$$

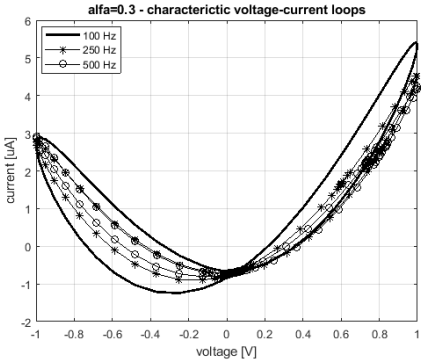
As can be seen (5) has the same structure as (1). The memristance and the flux are inversely proportional to each other. In other words, mathematical hysteresis curves in Fig. 3 can be obtained by using this circuit.

In order to verify the operation of the proposed circuit, it has been simulated using the SPICE macro models of the used active elements. Supply voltages are used

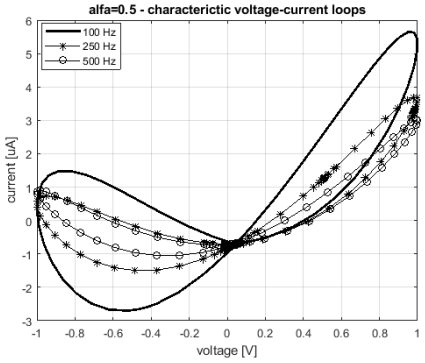
±10 V. The element values used in the simulation are given in Table 2. A frequency scaling coefficient as $k_f=(CR\beta)^{-1}$ is used for the FOI circuits. Obtained simulated pinched hysteresis loops are given in Fig. 6 with the input frequencies 100 Hz, 250 Hz and 500 Hz, for changing values of α. Simulated results are in good agreement with the theoretical results.

Table 2. Circuit parameters used in Fig. 6 proposed fractional order memristance simulator circuit.

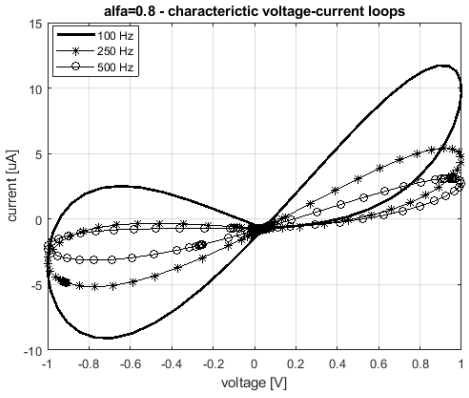
Element	R_1	R_2	R_3	R_4	k
Value	47 kΩ	10 kΩ	10 kΩ	194 kΩ	0.1 V^{-1}
At FOI circuit	Element	R_z	C_z	R_x	C_x
	Value for α=0.3	100 kΩ	100 nF	54 kΩ	54 nF
	Value for α=0.5	100 kΩ	100 nF	33 kΩ	33 nF
	Value for α=0.8	100 kΩ	100 nF	12 kΩ	12 nF



(a) α=0.3



(b) α=0.5

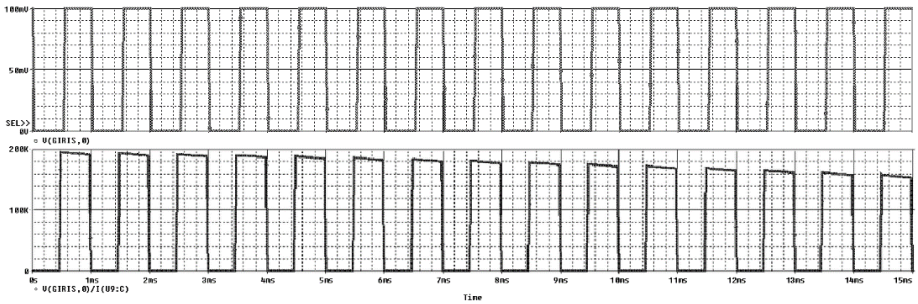


(c) α=0.8

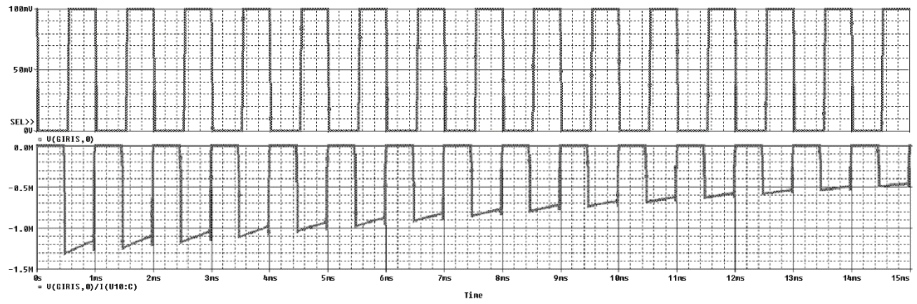
Fig. 6. Simulated characteristic pinched *v-i* hysteresis loops of fractional order memristor for changing α values

Another important feature of the memristor is the non-volatility feature. To show the non-volatility, square waves with a fixed amplitude of 100 mV, a period of

1 ms, and a pulse width of 0.5 ms have been applied to the positive and negative fractional order memristance simulator circuit, and the change of the memristance value has been observed with each pulse. When no voltage is applied to the element, it preserves the last memristance value, and when the voltage is applied again, the flux value starts to increase, the memristance value decreases inversely. The results obtained for the positive and negative simulator circuits are given in Fig. 7.



(a) Positive type fractional order memristance simulator



(b) Negative type fractional order memristance simulator

Fig. 7. Simulated waveforms when a pulse shaped voltage signal is applied to the simulator circuits (α=0.8)

5. An application example: simplest chaotic circuit

As shown in Fig. 8, the dynamic behaviour of a 3-element series *C-L-*M_f circuit is examined. Instead of the M_f element, the positive impedance simulator circuit given in Fig. 5a is connected as α = 0.5 order.

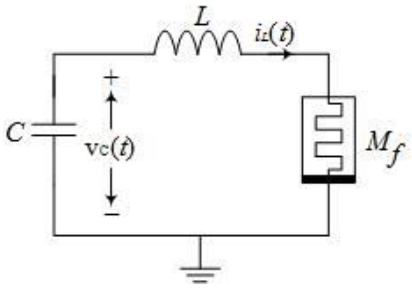


Fig. 8. Chaotic serial *C-L-*M_f circuit

While analyzing the circuit, using the integer order approximation of FOI, the ordinary differential equation set of the circuit was obtained as the first order. There are a total of four dynamic elements in the given series circuit, *C*, *L*, C_x and C_z. State equations of these four dynamic elements are obtained as in the next equations:

(6)
$$\frac{dV_C}{dt} = -\frac{i_L}{C},$$
$$\frac{di_L}{dt} = \frac{V_C}{L} - \frac{R_1}{R_3.L}.V_{Cx},$$
$$\frac{dV_{C_x}}{dt} = \frac{kR_4V_{C_x}^2}{R_x\left[(R_2+R_3).C_zi_L - kC_xR_4V_{C_x}\right]} - \frac{V_{C_z}kR_4V_{C_x}}{R_z\left[(R_2+R_3).C_zi_L - kC_xR_4V_{C_x}\right]} + \frac{(R_2+R_3).V_CC_z}{L\left[(R_2+R_3).C_zi_L - kC_xR_4V_{C_x}\right]} - \frac{(R_2+R_3).R_1V_CC_z}{R_3L\left[(R_2+R_3).C_zi_L - kC_xR_4V_{C_x}\right]},$$
$$\frac{dV_{C_z}}{dt} = \frac{V_{C_x}}{R_xC_z} - \frac{V_{C_z}}{R_zC_z} + \frac{C_x}{C_z}.\frac{dV_{C_x}}{dt}.$$

The first equation, the derivative of *C* capacitor voltage is obtained from the current equation $i_C+i_L=0$. The second equation, the derivative of *L* inductance current is obtained from the voltage equation, $-v_C+v_L+v_{M_f}=0$. The third and fourth equations are represent the fractional memristor element. They are derived from two equation. One of them is the $i_L+i_{M_f}=0$, when $i_{M_f}=kv_{C_x}v_{C_z}R_4/R_2R_3$. The other comes from the FOI circuit, $i_z=i_x$.

The bifurcation diagram of the proposed equation set is given in Fig. 9.

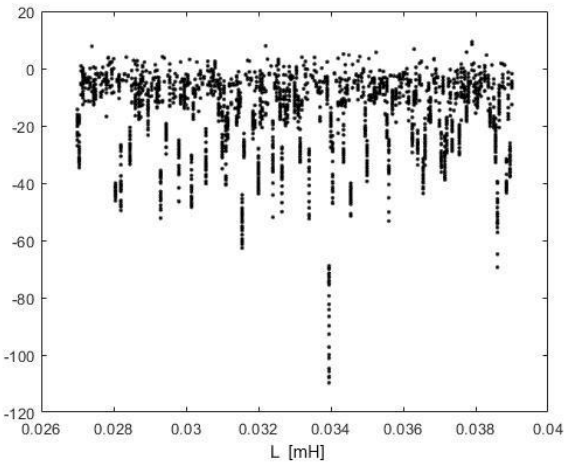
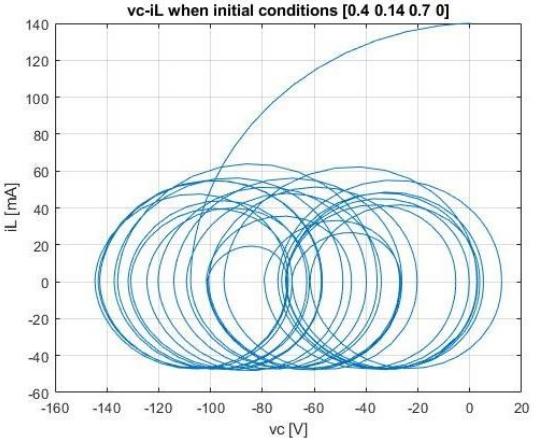
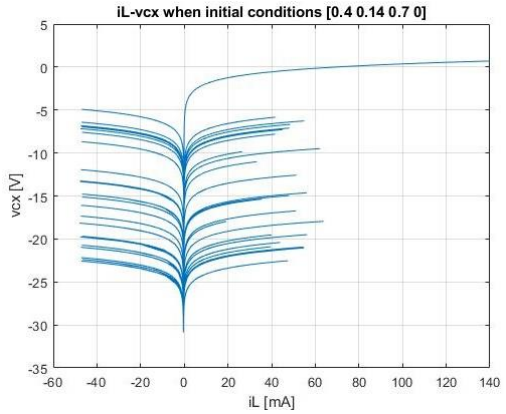


Fig. 9. Bifurcation diagram when *L* changes in a range of [27-39 mH]

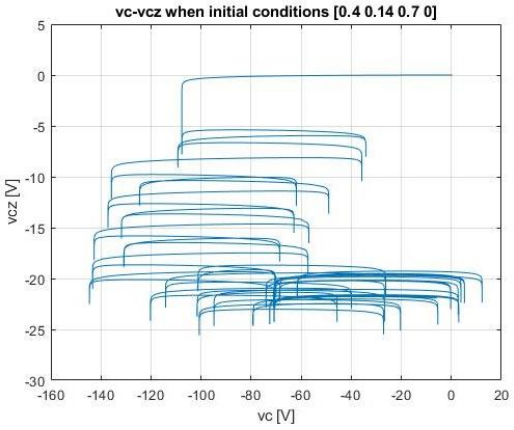
When this equation set is solved for 7 ms with the initial conditions [0.4 0.14 0.7 0], obtained phase portraits are given in Fig.10. This element creates new attractors with a simple serial circuit.



(a) v_C-i_L



(b) i_L-v_{Cx}



(c) v_C-v_{Cz}

Fig. 10. Mathematically obtained phase portraits

6. Conclusion

In this article, a new fractional-order memristance equation is derived and the mathematically obtained characteristic pinched *i-v* hysteresis loops are verified by SPICE simulations. An analog circuit is designed by using the commercially available integrated circuits and passive elements to physically perform this memristance equation. The designed circuit has floating structure. Both positive and negative memristance equations can be obtained with a small connection change in the circuit. A simple dynamic circuit example is given to show the behaviour of the proposed circuit. A new dynamic system that creates new attractors is examined mathematically.

One of the shortcomings in the literature is that not enough studies have been carried out on fractional order memristors. Emulator circuit studies are of great importance for the investigation of potential application areas of the memristor element since the solid-state fractional memristor has not been produced yet and the researchers have had insufficient studies on the implementation of fractional order memristor with arbitrary-order lattices, capacitors, memristors and inductors [29-30]. When one of the few studies on the fractional order memristor emulator in the literature is examined, the circuit proposed by Sanchez-Lopez and colleagues has no superiority over the proposed circuit in terms of the number of elements [28]. The fracmemristance equation in this study is similar to the integer order memristance relation described by HP which includes a constant and a flux-dependent term [31]. The simulator in the proposed study contains only a single term inversely proportional to the fractional order flux variable. Since it is suitable for positive or negative realization, it can be used to emulate an increasing or decreasing structure of fracmemistor with a resistance connected in series to the simulator. While investigating the use of the memristor element in hardware implementation of FONNs and performing fractional operations in learning algorithm circuits, it is thought that the proposed simulator circuit can be used.

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